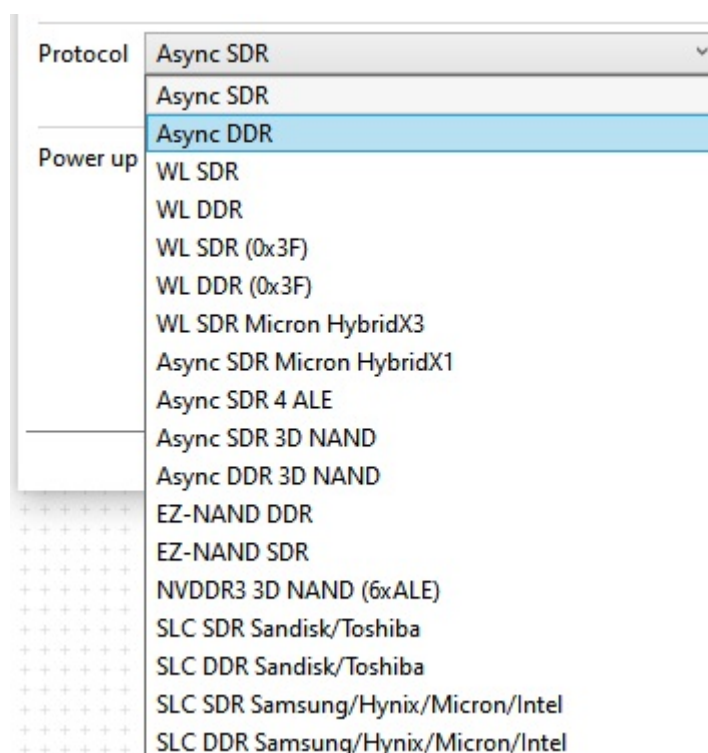




NAND Memory Protocols: The Difference Between SDR and DDR

Everyone who works in NAND data recovery knows that reading NAND requires using a protocol. The most popular protocols are Async and WL. Almost all protocols have two versions: SDR and DDR.



1. Protocols in reader configuration

What is SDR and DDR and what is the difference between them?

Difference Between SDR and DDR in NAND Memory:

SDR (Single Data Rate)

- Data Transfer Method:

Data is transferred on only one edge of the clock signal (RE), usually on the rising edge.

- **Data Transfer Speed:**

The data transfer speed in SDR mode is limited because data is transferred only once per clock cycle.

DDR (Double Data Rate)

- **Data Transfer Method:**

Data is transferred on both edges of the clock signal (RE) – both the rising and falling edges. This means twice as much data is transferred in each clock cycle.

- **Data Transfer Speed:**

The data transfer speed in DDR mode is twice as fast compared to SDR mode at the same clock frequency, leading to higher read and write performance.

It is possible for two devices to have the same NAND ID but use different read modes (SDR or DDR). This situation can occur due to several reasons:

- **Memory Controller Capabilities:**

The memory controllers in the devices may have different capabilities. One controller may support only SDR mode, while another, more advanced controller supports both SDR and DDR modes. This allows the same NAND chip to be used in different devices with varying performance requirements.

- **Design Requirements:**

The design requirements and intended use cases of the devices might differ. For instance, a high-performance SSD might use DDR mode to achieve faster data transfer rates, while a simpler, cost-effective device might use SDR mode to save on complexity and cost.

Example Scenario

Consider two different devices:

- **Device A:** A budget-friendly USB flash drive that uses SDR mode for reading data from the NAND flash. It focuses on cost-effectiveness and compatibility with a wide range of systems.
- **Device B:** A high-performance SSD that uses DDR mode to maximize data transfer speeds and provide better performance for data-intensive applications.

Both devices could use the same NAND flash chip with the same NAND ID, but their overall performance and use cases would differ significantly due to the different read modes enabled by their respective controllers and firmware.

How to Determine When It Is Necessary to Switch from SDR to DDR or from DDR to SDR

The answer lies in the bitmap. If the memory was using SDR mode, but the configuration in VNR is for DDR, then after opening the bitmap, we can see some characteristic patterns. In HEX mode, we can check if every byte is repeating twice. In that case, it is necessary to switch the protocol from DDR to SDR, for example, from Async DDR to Async SDR, WL DDR to WL SDR, and so on.

The screenshot displays a memory reader interface with two main panels. The left panel shows a grayscale bitmap of memory data. The right panel shows a hex dump of the same data. The hex dump is organized into columns labeled 00 through 0F. The data in the hex dump shows a repeating pattern of bytes, which is a characteristic sign that the memory is in SDR mode but configured for DDR. The interface also includes a status bar at the bottom with the address 638447616 and a selected range.

Byte position: 18; Row: 36130; Address: 638447616

Address: 638447616 Selected:

Event log explorer

Last active selection: address 638447616 selected

2. NAND using SDR reading by DDR mode

Let's check the reverse case: the NAND was using DDR mode, but the configuration in VNR is for SDR mode. The answer is also in the bitmap. The first thing we need to check is the first byte. If we are reading the memory in SDR mode, but the memory was used in DDR mode, then the first byte is almost always empty. However, this is not a rule for all cases. The second thing to check, and it always proves the reading mode is correct, is the middle of the page. If the memory was used in DDR mode, and we are reading it in SDR mode, we are reading only half of the bytes, and the data ends in the middle of the page, not near the end. In that case, we need to check how it looks when we change from SDR to DDR mode, and it is important to change from Async SDR to Async DDR or WL SDR to WL DDR. The rest of the protocol, except the reading mode (SDR/DDR), must remain the same.

The screenshot displays a memory reader application. On the left, a large, noisy bitmap represents the memory data. On the right, a hex dump shows the data in hexadecimal format. The address range shown is from 009F8FA000 to 009F8FA350. The interface includes a 'Reader 0 X' tab, a 'Workspace' area, and a status bar at the bottom showing 'Byte position: 26; Row: 145332; Address: 2676989953 Selected:'.

Address	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E
009F8FA000	00	8D	0A	66	73	D9	D3	E5	B7	31	0E	4E	1E	A3	FE
009F8FA010	7E	6A	2A	AA	7E	A3	8E	AB	4E	DA	00	48	AC	78	1C
009F8FA020	71	E5	01	8A	70	4A	24	39	D9	96	5C	23	63	D4	B0
009F8FA030	0D	ED	7D	EB	31	39	06	51	F6	CA	F8	22	41	96	5B
009F8FA040	7D	4D	3E	A1	48	DB	DC	87	90	BD	85	12	BA	10	F2
009F8FA050	92	BA	20	DA	53	3C	F3	20	EB	5A	8A	EB	2B	D3	B4
009F8FA060	EC	F9	35	97	ED	6E	88	5F	D8	E7	4D	92	88	0D	DC
009F8FA070	54	FA	2E	DB	41	FB	EB	34	F8	0D	DF	4E	3B	DC	B1
009F8FA080	16	69	05	5D	C4	99	08	42	18	61	F8	3F	D9	18	41
009F8FA090	F7	F4	51	17	DB	FB	C6	E4	CF	56	11	B9	61	D8	CE
009F8FA0A0	E8	D8	76	E4	E6	5A	AA	26	9D	55	AF	73	1D	48	B3
009F8FA0B0	9A	1C	5B	85	05	3D	7C	8B	AB	35	3F	E9	E9	83	04
009F8FA0C0	71	E1	A9	23	D7	B1	D7	54	C3	C9	4F	82	E1	40	7C
009F8FA0D0	F3	2B	49	4A	5F	5F	34	83	39	E4	BF	45	51	8D	2B
009F8FA0E0	3D	68	6D	09	51	60	69	89	A6	8C	D9	D4	73	14	74
009F8FA0F0	16	34	62	0F	68	EA	EF	ED	23	BB	7A	74	0D	C5	98
009F8FA100	8E	54	6A	B4	15	83	5B	38	0A	C8	AC	09	C7	50	7C
009F8FA110	5F	40	0B	77	09	01	5A	51	7E	DB	15	57	5A	F2	D0
009F8FA120	80	BF	93	8E	34	81	E7	17	72	F2	F4	87	29	5A	97
009F8FA130	98	32	21	0C	27	DA	10	46	CC	24	33	FF	47	9A	64
009F8FA140	5E	11	76	38	50	A5	64	18	CA	E7	BB	95	59	31	2B
009F8FA150	37	E0	25	EB	79	FD	93	64	DB	2A	99	5C	44	67	85
009F8FA160	42	D5	92	00	37	9E	A7	08	8C	9D	CE	ED	5E	23	2C
009F8FA170	96	C0	4D	B5	6B	EB	62	84	01	E5	EC	81	4D	0F	81
009F8FA180	3B	05	CC	04	D7	B2	6D	58	D6	E0	1A	0D	D0	93	38
009F8FA190	7B	54	A2	F9	BC	17	B9	87	5E	E1	B9	EE	91	01	01
009F8FA1A0	73	DF	8E	AE	F5	C2	79	6A	87	38	1F	7B	DE	15	E4
009F8FA1B0	CD	A5	5B	C1	49	F0	43	C6	30	3E	81	26	AC	8E	A4
009F8FA1C0	9F	4C	BF	AB	35	12	E8	04	F1	32	EE	B1	E1	3A	A1
009F8FA1D0	D2	47	CD	4F	6B	04	B1	EF	A0	D6	4E	35	48	FC	21
009F8FA1E0	3C	61	70	91	07	87	34	3F	D0	03	CE	E8	E9	F4	94
009F8FA1F0	85	65	24	C2	E4	33	52	51	B9	ED	F9	B4	3D	8B	A4
009F8FA200	93	22	76	A3	19	7D	6A	25	5B	56	98	D9	90	F3	31
009F8FA210	35	9E	EF	12	FE	9B	1E	D0	A1	0B	07	FD	D8	1F	F0
009F8FA220	77	8F	0E	D0	5C	5D	BF	7F	AF	55	82	0D	21	B3	9C
009F8FA230	A4	7C	FB	C9	74	07	35	B7	11	80	04	19	E3	01	34
009F8FA240	88	1F	CD	9C	31	A5	0F	9F	75	64	67	AD	2A	7C	E0
009F8FA250	A4	4A	2C	95	80	D3	68	E4	58	68	F7	CD	75	04	A1
009F8FA260	C0	16	0B	12	2B	FF	34	42	46	1E	09	DF	C5	4D	B1
009F8FA270	EB	47	0E	27	89	12	37	33	97	46	55	7E	9C	5C	13
009F8FA280	49	BB	93	D3	E5	99	61	32	E2	09	DC	E7	83	A5	90
009F8FA290	88	03	DA	12	0E	63	4C	C0	39	D1	9B	F9	52	9D	F8
009F8FA2A0	1D	4D	D5	32	34	98	8D	AA	89	85	A9	90	36	CB	7C
009F8FA2B0	84	6F	9F	59	BA	FF	61	6E	2C	30	0B	CD	B5	30	C4
009F8FA2C0	68	62	43	64	EF	0C	7F	E1	D7	26	D7	8F	45	28	23
009F8FA2D0	73	E7	05	59	73	BC	5A	B5	60	E9	0A	96	77	5E	30
009F8FA2E0	A2	7D	C4	E2	2E	70	5E	1E	14	40	E6	65	DC	58	30
009F8FA2F0	D9	79	D3	D7	AA	3E	E0	F5	FA	14	47	EA	54	B8	89
009F8FA300	B4	39	93	A8	BE	66	22	46	2C	13	B3	69	31	5E	61
009F8FA310	53	03	71	A5	9E	6C	0A	89	B8	7E	F1	40	67	A5	C2
009F8FA320	45	8B	FB	1E	3F	59	5C	48	27	D9	FD	77	8A	52	4C
009F8FA330	1F	43	29	FC	AE	B9	EA	AC	F7	37	49	CC	50	87	CF
009F8FA340	69	B6	21	E3	0F	0F	BD	DB	51	88	50	F5	B7	77	4E
009F8FA350	D9	BF	AA	93	B9	ED	B3	8A	32	54	01	B7	D4	E4	E0

3. NAND using DDR reading by SDR mode - begin of page

Reader 0 X Workspace

009F8FC260 00 01 02 03 04 05 06 07 08 09 0A 0B 0C 0D 0E 0F
 009F8FC270 D9 41 B0 4F 7E CA 91 08 B4 FF D0 0A F5 73 1C
 009F8FC280 EB AD AE 4A 84 95 E8 D6 C4 88 BD 25 93 9A 4C
 009F8FC290 73 2A 9B C2 D0 B5 F0 90 AD 16 93 C9 C7 22 09
 009F8FC2A0 7A 20 07 5A C9 C9 5F 79 DF 9D 4B E0 0A 24 56
 009F8FC2B0 C4 30 0E EE 63 97 0F D3 39 77 20 83 88 FF C4
 009F8FC2C0 C2 BF 22 EF A0 6A 40 14 92 60 35 92 49 42 09
 009F8FC2D0 D7 06 24 45 90 6D 5D F2 6D EC 31 47 3E 31 44
 009F8FC2E0 E4 09 31 4E 74 CA C4 AD DB BF 3C 7B 5B 87 4B
 009F8FC2F0 8B 19 17 F0 B2 51 EC 4C 87 51 65 28 E5 AC A2
 009F8FC300 D9 56 FD B1 72 94 78 E4 83 7B C8 58 01 DB C0
 009F8FC310 2A 59 9E 63 3F DD 44 B3 19 85 02 F0 5C 8F 20
 009F8FC320 C0 C1 71 8C 04 E3 CC 4E FE 65 19 0B 4F C1 62
 009F8FC330 A3 8A 0B 53 44 3B 7D D0 F7 27 3C 33 4C AF 42
 009F8FC340 BA EB 7E BF 9F E4 75 74 E1 C2 73 CB BD EA 58
 009F8FC350 9E BA 6F 94 F1 E3 FF E7 A1 61 41 5D C5 07 E8
 009F8FC360 F9 E9 F3 59 98 9B 98 55 57 6B 72 E1 A9 7F 18
 009F8FC370 F8 36 C4 AD EE 20 5A 8B 2F C5 A3 12 10 AF 09
 009F8FC380 77 8D A9 87 A2 09 FA 3F 42 DA C4 B5 6A 89 40
 009F8FC390 F5 86 78 5F 67 55 80 FC 57 40 CE 1E E0 3E 4B
 009F8FC3A0 A0 C6 D0 28 3D B0 E3 66 67 4A 30 F0 A9 E7 02
 009F8FC3B0 72 6C F3 68 8D A2 66 8C 6D D0 50 7D DA 4E B4
 009F8FC3C0 AC 30 BA A2 4F A0 36 09 D6 2E B0 C1 FA 7F 2B
 009F8FC3D0 03 06 84 8C 79 0F E7 61 AF D6 86 AD 00 B2 61
 009F8FC3E0 04 15 67 0E B6 4A C8 4D 7B C3 5A DB 47 68 D8
 009F8FC3F0 C1 D6 16 36 54 77 78 56 41 00 6C 78 C2 BA F8
 009F8FC400 A1 9D 0A 66 71 C9 30 48 13 C6 66 79 0B 92 B4
 009F8FC410 2D 00 00 00 00 00 00 00 00 00 00 00 00 00 00
 009F8FC420 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
 009F8FC430 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
 009F8FC440 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
 009F8FC450 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
 009F8FC460 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
 009F8FC470 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
 009F8FC480 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
 009F8FC490 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
 009F8FC4A0 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
 009F8FC4B0 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
 009F8FC4C0 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
 009F8FC4D0 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
 009F8FC4E0 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
 009F8FC4F0 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
 009F8FC500 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
 009F8FC510 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
 009F8FC520 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
 009F8FC530 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
 009F8FC540 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
 009F8FC550 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
 009F8FC560 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
 009F8FC570 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
 009F8FC580 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
 009F8FC590 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
 009F8FC5A0 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
 009F8FC5B0 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00

Byte position: 9208; Row: 145211; Address: 2676999161 Selected:

Event log explorer

Last active selection: address 2676999161 selected

4. NAND using DDR reading by SDR mode - middle of page

Let's Summarise

Sometimes it is possible to find the NAND configuration, but it is not possible to find ECC or XOR, or the solution from the database doesn't work. If the dump doesn't have bad columns, it is important to check the protocol mode used to read the memory as shown above.

